

08/31/00



JC921 U.S. PTO

9-5-00

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of: Gurtej Singh Sandhu et al.  
Title: METHOD FOR FORMING A METALLIZATION LAYER  
Attorney Docket No.: 303.085US4

JC796 U.S. PTO  
09/652619

08/31/00

**PATENT APPLICATION TRANSMITTAL****BOX PATENT APPLICATION**

Commissioner for Patents  
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

- ☒ Return postcard.  
☒ **CONTINUATION** of prior Patent Application No. 08/912,051 (under 37 CFR § 1.53(b)) comprising:  
☒ Specification ( 11 pgs, including claims numbered 1 through 20 and a 1 page Abstract).  
☒ Formal Drawing(s) ( 2 sheets).  
☒ Signed Combined Declaration and Power of Attorney ( 7 pgs).  
☒ Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*  
☒ Check in the amount of \$690.00 to pay the filing fee.  
☒ Prior application is assigned of record to Micron Technology, Inc.  
☒ Information Disclosure Statement ( 1 pgs), Form 1449 ( 1 pgs). References NOT enclosed, cited in prior application.  
☒ Preliminary Amendment ( 2 pgs).

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	1 - 20 =	0	x 18 =	\$0.00
INDEPENDENT CLAIMS	1 - 3 =	0	x 78 =	\$0.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				\$0.00
BASIC FEE				\$690.00
TOTAL				\$690.00

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: Daniel J. Kluth  
Atty: Daniel J. Kluth  
Reg. No. 32,146

Customer Number **21186**

"Express Mail" mailing label number: EL618477123US

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**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Gurtej Singh Sandhu et al.

Examiner: Unknown

Serial No.: Unknown

Group Art Unit: Unknown

Filed: Herewith

Docket: 303.085US4

Title: METHOD FOR FORMING A METALLIZATION LAYER

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**PRELIMINARY AMENDMENT**

Commissioner for Patents  
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

**IN THE SPECIFICATION**

On page 1, line 5, before "The present invention", please insert the sentence, --This application is a continuation of U.S. Serial No. 08/912,051 filed August 18, 1997 which is a continuation of U.S. Serial No. 08/656,712 now U.S. Patent No. 5,662,788.--

On page 3, line 5, please insert --Figures 2 and 3 are cross-sectional views of additional illustrative embodiments of the present invention.--

**IN THE CLAIMS**

Please cancel claims 2-20 without prejudice.

**REMARKS**

Currently claim 1 is pending in the application. Applicant will file additional claims in a Supplemental Preliminary Amendment. If the Examiner begins the examination without receiving the new claims, it is respectfully requested that the Examiner contact the below signed attorney to receive a copy of the new claims.

**PRELIMINARY AMENDMENT**

Serial Number: Unknown

Filing Date: Herewith

Title: METHOD FOR FORMING A METALLIZATION LAYER

**Page 2**

D.t.: 303.085US4

Respectfully submitted,

GURTEJ SINGH SANDHU ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6904

Date Aug. 31, 2000 By Daniel J. Kluth  
Daniel J. Kluth  
Reg. No. 32,146

"Express Mail" mailing label number: EL618477123US

Date of Deposit: August 31, 2000

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## Method for Forming a Metallization Layer

### Technical Field of the Invention

5           The present invention relates generally to integrated circuits and, in particular, to a method for forming a metallization layer.

### Background of the Invention

10           An integrated circuit comprises a large number of semiconductor devices, such as transistors, that are formed on a semiconductor substrate or, more colloquially, a "chip." These devices are selectively interconnected by one or more patterned layers of a conductive material, typically aluminum, to form a circuit that performs a desired function. These layers are referred to as "metallization" layers. As integrated circuits become more complex, designers reduce the minimum feature size of the constituent  
15           devices of the circuit, so as to fit more devices on a chip. With this reduction in size, it becomes more difficult to achieve proper pattern definition using conventional techniques such as photolithography and dry etch techniques for forming metallization layers. Further, designers have attempted to use copper instead of aluminum as the principle metallization material in the metal-lization layers, due to perceived advantages  
20           in resistivity, ductility and melting point. Unfortunately, developers have not been able to create a reliable technique for patterning a copper layer.

          For example, one process using electro-deposition for forming a copper metallization layer is described in U.S. Patent No. 5,151,168. According to this process, a conductive barrier layer is deposited on a semiconductor substrate. Further, a  
25           photoresist reverse image of the maskwork normally used to etch the metallization pattern is created on the substrate. The wafer is then transferred to an electrolytic bath in which the copper is complexed with EDTA molecules. A fixed voltage is applied between a voltage source and the semiconductor substrate to deposit the copper ions on the barrier layer that is not covered by the photoresist layer including contact/via  
30           openings on the semiconductor substrate. Unfortunately, when the substrate is placed in

the electrolytic bath, the photoresist material may lift-off from the substrate thus depositing copper in areas where it is not required.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a method for forming a metallization layer  
5 that avoids the disadvantages and problems of prior techniques.

### Summary of the Invention

A method for forming a metallization layer is described which uses a single  
10 electro-deposition step to reliably form both the metallization layer and to fill the contact vias. In particular, one embodiment of the present invention uses first and second layers of materials that are placed at different surface potentials to form the metallization layer. The first layer is formed outwardly from a semiconductor substrate. Contact vias are formed through the first layer to the semiconductor substrate. The  
15 second layer is formed outwardly from the first layer. Portions of the second layer are selectively removed such that the remaining portion of the second layer defines the layout of the metallization layer and the contact vias. Metal ions in a solution are electro-deposited by applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle to the layers and the solution. The voltage and surface  
20 potentials are selected such that the metal ions are deposited on the remaining portions of the second layer. Further, metal ions deposited on the first layer during a positive duty cycle are removed from the first layer during a negative duty cycle. Finally, exposed portions of the first layer are selectively removed.

In another embodiment of the present invention, the first and second layers are  
25 placed at different surface potentials by applying a first voltage to a surface of the first layer and applying a second voltage, higher than the first voltage, to the second layer. In another embodiment of the present invention the different surface potentials are achieved in part by selecting materials for the first and second layers that have different innate surface potentials.

### Brief Description of the Drawings

Figures 1A through 1D are cross-sectional views of a semiconductor substrate that illustrate process steps according to an illustrative embodiment of the present invention.

5

### Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These  
10 embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be used and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

15 Figures 1A through 1D are cross-sectional views of semiconductor substrate 10 that depict process steps according to an illustrative embodiment of the present invention. Advantageously, the illustrative embodiment forms a metallization layer, including filling contact vias, outwardly from semiconductor substrate 10 in a single electro-deposition step. The process exposes adjacent layers of materials that are  
20 formed outwardly from semiconductor substrate 10 with different surface potentials to a bi-polar modulated voltage source to deposit the metallization layer and to fill the contact vias. The surface potentials and the modulated voltage are selected such that the metallization layer forms only on the second layer because metal that deposits on the first layer during a first duty cycle of the bi-polar modulated voltage is removed from  
25 the first layer during a second duty cycle.

As shown in Figure 1A, borophosphosilicate glass (BPSG) layer 12 is deposited and reflowed outwardly from semiconductor substrate 10. First layer 14 is formed outwardly from BPSG layer 12. First layer 14 may comprise, for example, poly-silicon, doped or undoped, that is deposited using a conventional chemical vapor deposition

(CVD) or sputtering technique. Alternatively, other materials such as germanium may be substituted for the poly-silicon. Contact via 16 is etched through first layer 14 and BPSG layer 12 to, for example, junction 18 of semiconductor substrate 10. Second layer 20 is formed outwardly from first layer 14 so as to line contact via 16 and cover first layer 14 by, for example, depositing a layer of titanium nitride or other appropriate barrier layer material using a conventional sputter or chemical vapor deposition technique. First layer 14 and second layer 20 have a thickness on the order of 100 to 500 Å. Advantageously, the innate surface potential of first layer 14 is lower than the innate surface potential of second layer 20. This difference in surface potentials contributes to the selectivity of the electro-deposition step described below. In other embodiments, first and second layers 14 and 20 can be fabricated from other materials that provide similar differences in innate surface potential.

Portions of second layer 20 are selectively removed such that the remaining portions of second layer 20 match the desired pattern for the metallization layer, including contact vias. As shown in Figure 1B, layer 22, comprising, for example, a conventional photoresist material, is formed outwardly from layer 20 using conventional techniques. Layer 22 is exposed through a mask. Portions of layer 22 are removed with a solvent so as to produce a patterned layer of photoresist material that matches the desired metallization layer. The exposed portions of layer 20 are removed with, for example, a dry etch leaving a patterned version of layer 20. Layer 22 is removed.

Once layer 20 is patterned, semiconductor substrate 10 is placed in an electrolytic bath for electro-deposition of the metallization layer outwardly from layer 20 so as to fill contact vias 16. The bath includes metal ions in a solution. For example, the metal ions may comprise copper ions in a solution as described in U.S. Patent No. 5,151,168 entitled "Process for Metallizing Integrated Circuits With Electrically-Deposited Copper" (the "'168 Patent"), the teachings of which are incorporated by reference. Specifically, one embodiment of the electrolytic bath is described in the '168

Patent at Column 5, lines 10 through 35. Alternatively, the electrolytic bath may comprise a solution containing nickel or palladium ions.

Voltage source 26 provides a bipolar modulated voltage to anode 28 and voltage source 24 provides a DC offset voltage to anode 28. The voltage on anode 28 causes metal ions to be deposited on a layer when the potential difference between anode 28 and the surface potential of the layer exceeds the reduction potential of the metal. Conversely, the voltage on anode 28 causes metal ions to be removed from the surface of a layer when the potential difference between anode 28 and the surface potential of the layer is less than the reverse deposition potential of the metal. The voltages of sources 26 and 28 are selected such that metal deposited on layer 14 during a first duty cycle is removed during a second duty cycle. Further, metal is not removed from layer 20 during the second duty cycle. For example, in one embodiment source 26 provides a square wave with a dc offset provided by source 24 such that during the positive duty cycle of source 26, metal ions deposit on layers 14 and 20 and during the negative duty cycle copper is etched from layer 14. In other embodiments, source 26 comprises other time-varying wave-forms such as a triangle wave, sinusoidal wave or other appropriate voltage wave form.

Once the deposition of metallization layer 30 is complete, exposed portions of first layer 14 are removed leaving the structure shown in Figure 1D. In one embodiment, metallization layer 30 covers all of the exposed surfaces of layer 20 as shown in Figure 2. It is understood that an integrated circuit constructed according to this process would include a complete metallization layer with a plurality of contact vias even though only portions of the metallization layer and a single contact via are shown in Figures 1A through 1D.

25

### Conclusion

Although an illustrative embodiment has been described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown.

This application is intended to cover any adaptations or variations of the illustrative embodiment. For example, the type of modulated voltage can be varied from the specified square wave used in the illustrative embodiment. Further, the difference in surface potential between layers 14 and 20 can be imposed or enhanced by applying  
5 voltages to the surfaces of layers 14 and 20. In this embodiment, layers 14 and 20 are separated by insulating layer 15 as shown in Figure 3. The composition of the electrolytic bath can be varied so long as metal ions deposit on layer 20 when sources 24 and 26 are applied to anode 28.

What is claimed is:

1. A method for forming a metallization layer outwardly from a semiconductor substrate, the method comprising the steps of:
  - 5 forming a first layer of a material outwardly from the semiconductor substrate; forming contact vias that extend through the first layer to the semiconductor substrate;
  - forming a layer of a second material outwardly from the first layer;
  - selectively removing portions of the second layer such that the remaining
  - 10 portion of the second layer defines the layout of the metallization layer and the contact vias;
  - placing the first and second layers at different surface potentials;
  - electro-depositing the first and second layers in a solution of metal ions by applying a bi-polar modulated voltage having a positive duty cycle and a negative duty
  - 15 cycle, the voltage and surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and
  - selectively removing exposed portions of the first layer.
- 20 2. The method of claim 1, wherein the step of depositing a first layer comprises depositing a layer of poly-silicon outwardly from the semiconductor substrate.
3. The method of claim 1, wherein the step of electroplating comprises the steps of:
  - depositing the semiconductor substrate in an electrolytic bath containing a metal
  - 25 having a reduction potential; and
  - exposing the bath to a modulated voltage such that during a positive duty cycle the metal is deposited on exposed surfaces of the first layer and the second layer and that during a negative duty cycle the metal is removed from the exposed surface of the first layer.

4. The method of claim 1, wherein the step of depositing a second layer comprises depositing a layer of titanium nitride.

5. The method of claim 3, wherein the step of depositing the semiconductor  
5 substrate in an electrolytic bath comprises the step of depositing the semiconductor substrate in an electrolytic bath containing copper ions.

6. The method of claim 1, wherein the step of placing the first and second layers at  
different surface potentials comprises the step of applying a first voltage to a surface of  
10 the first layer and applying a second voltage, different than the first voltage, to the second layer, wherein the first and second layers are separated by an insulating layer.

7. The method of claim 1, wherein the step of placing the first and second layers at  
different surface potentials comprises the step of selecting a material for the first layer  
15 that has an innate surface potential that is less than the innate surface potential for the material selected for the second layer.

8. The method of claim 1, wherein the step of electroplating the first and second  
surfaces comprises the step of electroplating the first and second surfaces with a voltage  
20 source that produces a substantially square wave voltage output.

9. A method for forming a metallization layer outwardly from a semiconductor  
substrate, the method comprising the steps of:  
forming a first layer of a material outwardly from the semiconductor substrate,  
25 the first layer having a first innate surface potential;  
forming contact vias that extend through the first layer to the semiconductor  
substrate;

forming a layer of a second material outwardly from the first layer so as to line the contact vias and cover the first layer, the second layer having a second innate surface potential different from said first innate surface potential;

selectively removing portions of the second layer such that the remaining  
 5 portion of the second layer defines the layout of the metallization layer and the contact vias;

placing the semiconductor substrate with the first and second layers in an electrolytic bath comprising a solution of metal ions;

applying a bi-polar modulated voltage having a positive duty cycle and a  
 10 negative duty cycle to the electrolytic bath, the voltage and surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and

selectively removing exposed portions of the first layer.  
 15

10. The method of claim 9, wherein the step of depositing a first layer comprises depositing a layer of poly-silicon outwardly from the semiconductor substrate.

11. The method of claim 9, wherein the step of placing the semiconductor substrate  
 20 with the first and second layers in an electrolytic bath comprises the step of placing the semiconductor substrate with the first and second layers in an electrolytic bath containing copper ions in solution.

12. The method of claim 9, wherein the step of depositing a second layer comprises  
 25 depositing a layer of titanium nitride.

13. The method of claim 9, and further comprising the step of imposing an external voltage to one of the first and second layers to place the first and second layers at different surface potentials.

14. The method of claim 9, and further comprising the step of placing the first and second layers at different surface potentials by applying a first voltage to a surface of the first layer and applying a second voltage, different from the first voltage, to the second layer, wherein the first and second layers are separated by an insulating layer.

5

15. The method of claim 9, wherein the step of electroplating the first and second surfaces comprises the step of electroplating the first and second surfaces with a voltage source that produces a substantially square wave voltage output.

10 16. An integrated circuit, comprising:

a plurality of semiconductor devices formed on a semiconductor substrate;

a metallization layer formed outwardly from the semiconductor substrate that selectively interconnects the semiconductor devices so as to be operable to perform a function;

15 a first patterned layer of material formed outwardly from the semiconductor substrate that matches the metallization pattern; and

a second patterned layer of material, formed between the metallization layer and the first patterned layer, that matches the metallization pattern and lines contact vias that extend through the first layer to the semiconductor substrate.

20

17. The integrated circuit of claim 16, wherein the metallization layer comprises copper deposited on the second layer in an electrolytic bath.

18. The integrated circuit of claim 16, wherein the first layer comprises poly-silicon.

25 19. The integrated circuit of claim 16, wherein the second layer comprises titanium nitride.

20. The integrated circuit of claim 16, wherein the metallization layer comprises copper.

**Abstract of the Disclosure**

A method for forming a metallization layer (30). A first layer (14) is formed outwardly from a semiconductor substrate (10). Contact vias (16) are formed through the first layer (14) to the semiconductor substrate (10). A second layer (20) is formed outwardly from the first layer (14). Portions of the second layer (20) are selectively removed such that the remaining portion of the second layer (20) defines the layout of the metallization layer (30) and the contact vias (16). The first and second layers (14) and (20) are electroplated by applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle to the layers in a solution containing metal ions. The voltage and surface potentials are selected such that the metal ions are deposited on the remaining portions of the second layer (20). Further, metal ions deposited on the first layer (14) during a positive duty cycle are removed from the first layer (14) during a negative duty cycle. Finally, exposed portions of the first layer (14) are selectively removed.

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FIG. 1A

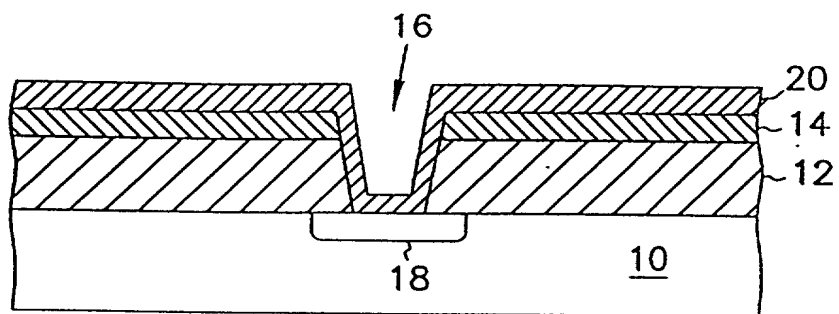


FIG. 1B

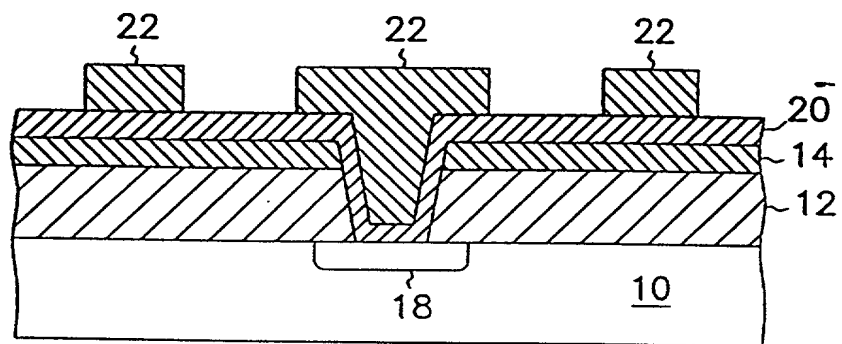


FIG. 1C

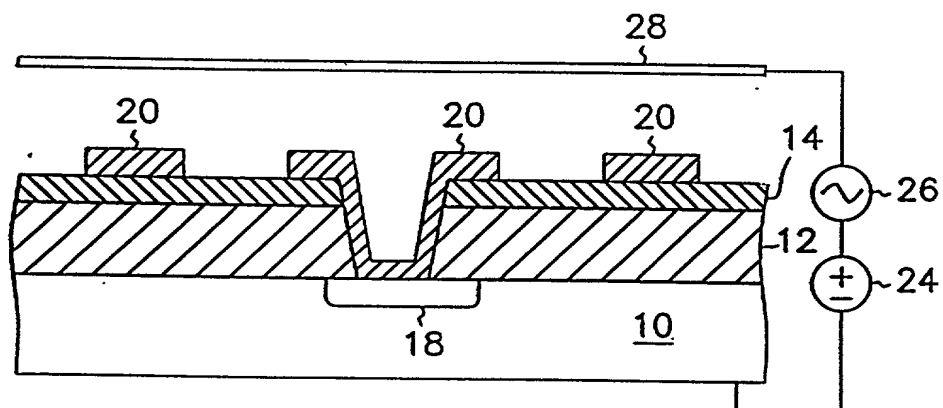


FIG. 1D

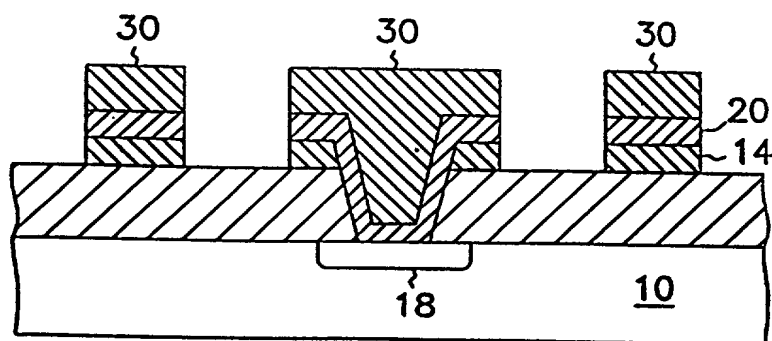


FIG. 2

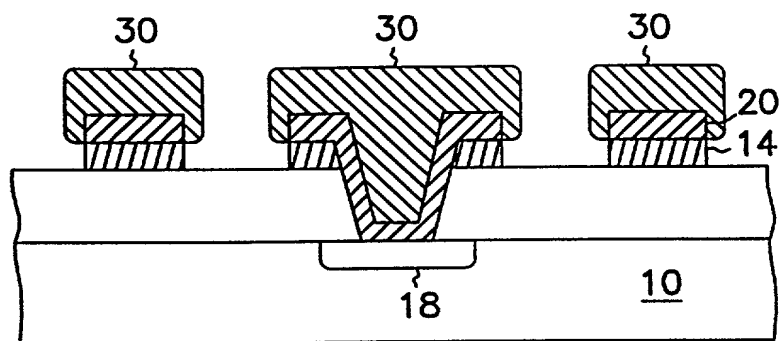
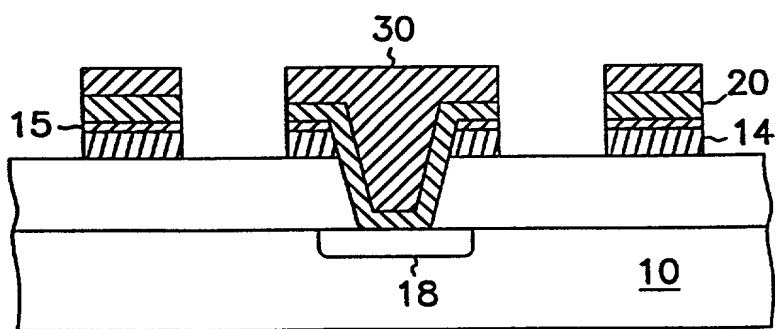


FIG. 3



SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

# United States Patent Application

## COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: METHOD FOR FORMING A METALLIZATION LAYER.

The specification of which

a. ☒ is attached hereto

b. ☐ was filed on \_\_\_\_\_ as application serial no. \_\_\_\_\_ and was amended on \_\_ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. \_\_ filed \_\_ and as amended on \_\_ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications have been filed.

b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in

Our Ref: 303.85US1

Page 2 of 4

Title: Method for Forming a Metallization Layer

Filing Date: Herewith

the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

US APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS(patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billig, Patrick G.	Reg. No. 38,080	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Brennan, Thomas F.	Reg. No. 35,075	Forrest, Peter	Reg. No. 33,235	Schwegman, Micheal L.	Reg. No. 25,816
Burke, John E.	Reg. No. 35,836	Holloway, Sheryl S.	Reg. No. 37,850	Slifer, Russell D.	Reg. No. 39,838
Clark, Barbara J.	Reg. No. 38,107	Kalinowski, Leonard J.	Reg. No. 24,207	Viksnins, Ann S.	Reg. No. 37,748
Dennison, Lia Pappas	Reg. No. 34,095	Kluth, Daniel J.	Reg. No. 32,146	Woessner, Warren D.	Reg. No. 30,440
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198		
Farney, W. Bryan	Reg. No. 32,651	Lempia, Bryan J.	Reg. No. 39,746		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

201	Full Name of Inventor	Family Name	First Given Name	Second Given Name
		SANDHU	Gurtej	Sandhu
	Residence & Citizenship	City	State or Foreign Country	Country of Citizenship
		Boise	Idaho	Great Britain
	Post Office Address	Post Office Address	City	State & ZipCode/Country
		2964 East Parkriver Drive	Boise	Idaho 83706/USA
202	Full Name of Inventor	Family Name	First Given Name	Second Given Name
		YU	Chris	Chang
	Residence & Citizenship	City	State or Foreign Country	Country of Citizenship
		Boise	Idaho	USA
	Post Office Address	Post Office Address	City	State & ZipCode/Country
		2801 Stewart Avenue	Boise	Idaho 83702/USA
203	Full Name of Inventor	Family Name	First Given Name	Second Given Name
	Residence & Citizenship	City	State or Foreign Country	Country of Citizenship
	Post Office Address	Post Office Address	City	State & ZipCode/Country
Signature of Inventor 201		Signature of Inventor 202	Signature of Inventor 203	
Date 5/23/96		Date	Date	

For Additional Inventors: \_\_ Indicate here and attach sheet with same information, including date and signature.

**§ 1.56 Duty to disclose information material to patentability.**

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
- (2) It refutes, or is inconsistent with, a position the applicant takes in:
  - (i) Opposing an argument of unpatentability relied on by the Office, or
  - (ii) Asserting an argument of patentability.

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(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
- (2) Each attorney or agent who prepares or prosecutes the application; and
- (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

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# United States Patent Application

## COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: METHOD FOR FORMING A METALLIZATION LAYER.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

### Application Number

### Filing Date

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

### Application Number

### Filing Date

### Status

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Farney, W. Bryan	Reg. No. 32,651	Lempia, Bryan J.	Reg. No. 39,746
Billig, Patrick G.	Reg. No. 38,080	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billion, Richard E.	Reg. No. 32,836	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Breanan, Thomas F.	Reg. No. 35,075	Forrest, Peter	Reg. No. 33,235	Schwegman, Micheal L.	Reg. No. 25,816
Burke, John E.	Reg. No. 35,836	Holloway, Sheryl S.	Reg. No. 37,850	Slifer, Russell D.	Reg. No. 39,838
Clark, Barbara J.	Reg. No. 38,107	Kalinowski, Leonard J.	Reg. No. 24,207	Viksnins, Ann S.	Reg. No. 37,748
Dryja, Michael A.	Reg. No. 39,662	Kluth, Daniel J.	Reg. No. 32,146	Woessner, Warren D.	Reg. No. 30,440
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : Gurtej Singh Sandhu  
Citizenship: Great Britain  
Post Office Address: 2964 East Parkriver Drive  
Boise, ID 83706

Residence: Boise, ID

Signature: \_\_\_\_\_ Date: \_\_\_\_\_  
Gurtej Singh Sandhu

Full Name of joint inventor number 2 : Chris Chang Yu  
Citizenship: United States of America  
Post Office Address: 255 North Oakhurst Drive  
Apt. 33  
Aurora, IL 60504

Residence: Aurora, IL

Signature: Chris Chang Yu Date: May 25, 1996  
Chris Chang Yu

Full Name of inventor:  
Citizenship:  
Post Office Address:

Residence:

Signature: \_\_\_\_\_ Date: \_\_\_\_\_

Full Name of inventor:  
Citizenship:  
Post Office Address:

Residence:

Signature: \_\_\_\_\_ Date: \_\_\_\_\_

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